THE IMPACT OF HIGH RESONANT FREQUENCY IN INVERTER APPLICATION

By

NIZAR BIN ABDUL NAZER

FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF APPROVAL

THE IMPACT OF HIGH RESONANT FREQUENCY IN INVERTER APPLICATION

by

Nizar Bin Abdul Nazer

A project dissertation submitted to the
Electrical & Electronics Engineering Programme
Universiti Teknologi PETRONAS
in partial fulfilment of the requirement for the
BACHELOR OF ENGINEERING (Hons)
(ELECTRICAL & ELECTRONICS ENGINEERING)

Approved By:

_____	_____
Pn. Khairul Nisak Bt M. Hasan	Nor Zaihar Yahaya
Project Supervisor	Project Co-Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

JUNE 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

_____

Nizar Bin Abdul Nazer

ABSTRACT

This project is mainly about the study of resonant frequency in a converter system. The inverter circuit is also considered as a type of resonant converter. Inverter circuit goes through inversion process where inverter has additional stage that is the resonant stage where the DC signal is converted to high-frequency AC signal. The main objective of this project is to analyze the effect of resonant frequency greater than switching frequency ($f_r > f_s$) when this condition is varied. A switching frequency of 20 kHz is generated through voltage pulses in a full bridge RCL inverter circuit. The condition of the circuit is monitored when the resonant frequency of the circuit being varied through simulation using PSPICE. The simulation results will be analyzed based on the performance of current and voltage in the circuit. There are four different resonant frequencies used for comparison purpose. The results are analyzed and effects of resonant frequency higher than switching frequency will be clarified according to the circuit performance and the applications. The best condition varied through the simulation analysis is when the resonant frequency is 50 kHz. High resonant frequency contributes to reducing switching loss.

ACKNOWLEDGEMENTS

Final Year Project has been such a challenging yet satisfying experience for me as the author of the project. Firstly, I am grateful for GOD as giving me the strength and opportunity to complete my final year project. I would like to show my appreciation to the project co-supervisor, Mr Nor Zaihar Yahaya for helping me throughout this one year by giving guidance, ideas and motivation. His helpful guidance with tenacious supervision, also patience to make me understand deserves a special mention. Without his expertise in my field of study that is Power Electronics, I can never complete the project. I also would like to express gratitude to my supervisor Pn Khairul Nisak who had helped me giving ideas and support me in completing this project. Special thanks to the FYP committee that help to give guideline in order to complete the project. Not to forget, all the lab technicians that had assist in technical practical expertise since. Last but not least, prayer from my dearest parent helps me a lot to keep focus and can cope with the challenge in completing this project.

TABLE OF CONTENTS

LIST OF TABLES viii
LIST OF FIGURES ix
LIST OF ABBREVIATIONS xi
CHAPTER 1 INTRODUCTION 1
1.1 Background of Study 1
1.2 Problem Statement 3
1.3 Objective and Scope of Study 3
CHAPTER 2 LITERATURE REVIEW 4
2.1 Theory 4
2.2 Resonant Power Converter 5
2.2.1 Losses in Power Converter 6
2.3 Inverter Concept 10
2.3.1 Basic Inverter Circuit 11
2.3.2 Phase shift-PWM full bridge inverter 12
2.3.3 Full Bridge Series-Parallel Resonant Inverter 13
2.3.4 Full bridge Inverter with Resistive and Inductive load 15
2.4 Gate Pulse Implementation 16
2.5 Step Response of Series RCL Circuit 17
CHAPTER 3 METHODOLOGY 19
3.1 Procedure Identification 19
3.2 Analysis Techniques 20
3.3 Tools and Equipment Required 27
CHAPTER 4 RESULTS AND DISCUSSIONS 28
4.1 Simulation Results and Analyses 28
CHAPTER 5 CONCLUSION AND RECOMMENDATION 39
5.1 Conclusion 39
5.2 Recommendation 39
REFERENCES 40
APPENDICES 42
Appendix A gantt chart FYP 1 43
Appendix B gantt chart FYP 2 45

Appendix C datasheet-irf 150 datasheet 47
Appendix D results for switching loss (*I-V* interception) 53

LIST OF TABLES

Table 1: Parameters for Full Bridge Inverter Circuit with RCL Load ($f_s>f_r$)…….....23

Table 2: Parameters for Full bridge Inverter Circuit with RCL Load ($f_s<f_r$)……24

Table 3: Parameters for Full Bridge Inverter circuit with RCL load ($f_s<f_r$)……..24

Table 4: Parameters for Full Bridge Inverter circuit with RCL load ($f_s<f_r$)……..25

Table 5: Inductor Current Comparison……..36

LIST OF FIGURES

Figure 1: Block diagram of a power electronic system……1

Figure 2: Voltage and current waveforms at two different frequencies…… 4

Figure 3: Ideal Switching Loss (*I-V*)……...6

Figure 4:Effects to current and waveform when varying f_s..... 7

Figure 5:Dead Time Interval in PWM Switching……... 10

Figure 6: Half- bridge inverter circuit with large splitting capacitor..... 11

Figure 7: Full bridge inverter with series load resonant …… 12

Figure 8(a): Operating frequency lower than resonant frequency …… 13

Figure 8(b): Operating frequency higher than resonant frequency …… 13

Figure 9(a): Resonant inverter circuit …… 14

Figure 9(b): Simplified resonant tank…… 14

Figure 10: Full Bridge Inverter with Resistive and Inductive Load ……..... 15

Figure 11: Voltage and Current Output Waveform……... 16

Figure 12: PWM gate pulse sequences……16

Figure 13: Project work flow diagram…… 19

Figure 14: Full Bridge Inverter with RCL Load in Series……..…….... 20

Figure 15: Setting for pulse generator……23

Figure 16: Operating Waveform of V_{gs} for M1, M2, M3 and M4 MOSFETs…..... 26

Figure 17: waveform of V_{gs1} and V_{gs2}…… 26

Figure 18: Output Voltage and Current for Full Bridge Inverter with RCL Load…. 28

Figure 19: operation waveforms for f_r = *4.78kHz*..... 29

Figure 20 :Output Waveform for f_r=*4.78kHz*……..... 30

Figure 21: operation Waveforms for f_r = *30kHz*…… 31

Figure 22 : Output Waveform for f_r=*30kHz*…….. 32

Figure 23: operation Waveforms for f_r = *50kHz*…… 33

Figure 24 : Output Waveform for f_r=*50kHz*……... 34

Figure 25: operation Waveforms for f_r = *100kHz*…….. 34

Figure 26 : Output Waveform for f_r=*100kHz*…… 35

Figure 27: graph of resonant frequency vs inductor current……... 36

Figure 28(a): Output Waveform during M1 turn-off……...37
Figure 28(b): Output Waveform during M2 turn-on……. 38

LIST OF ABBREVIATIONS

DC	- Direct Current
AC	- Alternate Current
PWM	-Pulse Width Modulator
EMI	-Electromagnetic Interferences
L	-Inductor
C	-Capacitor
SRC	-Series Resonant Parallel
ZVS	-Zero Voltage Switching
ZCS	-Zero Current Switching
MOSFET	-Metal Oxide Semiconductor Field Effect Transistor
IGBT	-Insulated Gate Bipolar Transistor
BJT	-Bipolar Junction Transistor
ESL	-Effective Series Inductance
ESR	-Effective Series Resistance

CHAPTER 1
INTRODUCTION

.

1.1 Background of Study

The proposed topic only covers the analysis of the conversion system. The conversion system is most likely to be DC to high frequency AC inverter [1]. It is also a type of resonant converter. The function of power conversion stage is to perform the actual power conversion and processing the energy from the input to the output by incorporating a matrix of power switching devices. The control of the output power is carried out through control signals applied to these switching devices. As to simplify the above matter, power conversion refers to changes in voltage form (AC or DC), voltage level (magnitude), voltage frequency etc [4]. Figure below shows the block diagram of power electronic system.

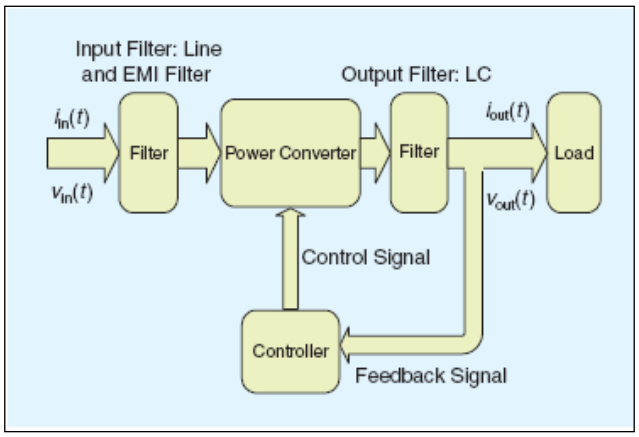


Figure 1: Block diagram of a power electronic system [3]

The power converter section in above block diagram refers to four conversion circuits that are used in today's power electronic circuit:

1. AC to AC (Cycloconversion)
2. AC to DC (Rectification)
3. DC to AC (Inversion)
4. DC to DC (conversion)

The topic proposed refers to inversion concept. In last few years, resonant-link technology that has been successful in the design of PWM power supplies has been applied to the design of DC to AC inverters, producing AC outputs at variable voltage and frequencies. PWM is the improvement from the first generation converter; however PWM switching still has several limitations. Thus the third generation was introduced in late 1980s known as resonant converter [2].

The advantages of this resonant converter compared with the others are that it reduce power losses, thus achieving high switching frequency and high power density while maintaining high efficiency. Today's resonant converter techniques are used in design of both high-frequency DC-DC conversion and high-frequency DC-AC inversion. [1]

1.2 Problem Statement

Various studies have been done in order to reduce the switching loss while maintaining the performance of the circuit. Resonant converter was chosen because of its ability to reduce the switching losses in circuit .However we cannot actually prove the best condition for the resonant converter. Therefore, this project will analyze the condition of resonant frequency bigger than switching frequency to serve the best condition to the resonant circuit while still paying attention to the external condition of the circuit such as the condition of output voltage, duty cycle and dead time effects.

1.3 Objective and Scope of Study

The main objectives of this project are as follow:

1. To prove that resonant frequency greater than switching frequency ($f_r > f_s$) condition serves the best for the resonant converter circuit
2. To briefly describe about the condition and the effect to the converter circuit when the resonant frequency is varied.

The scope of study for this project is to study the effect of resonant frequency in resonant converter in order to improve the efficiency of the system. The resonant converter will be represented by simulation using PSPICE for analysis. Once all properties of the component in the circuit being defined, the simulation will be started by varying the resonant frequency and switching frequency. Finally, the simulation will be analyzed and compared. From the results the conclusion will be drawn.

CHAPTER 2
LITERATURE REVIEW

2.1 Theory

Switching frequency (f_s) is defined as one cycle of on-time (t_{on}) and off-time (t_{off}) of the device. It can be representing as $f_s = \frac{1}{T_s}$ where T_s is the switching time. Resonant frequency (f_r) is when the inductive reactance (X_L) and capacitive reactance (X_C) is equal in absolute value and can be represented as $f_r = \frac{1}{2\pi\sqrt{LC}}$ where L is the inductive value and C is the capacitive value [2].

In power converter, switching frequency plays a big role in manipulating the current and voltage of the inductive load. The switching frequency depends on the cycle time [3]. As you can see in the figure 2 below different switching frequency shows different output of current and voltage for inductive load.

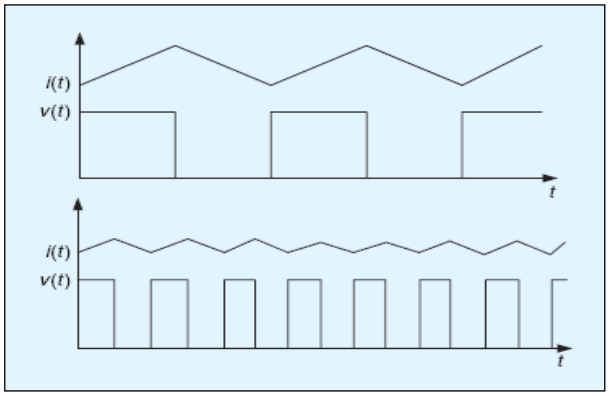


Figure 2: voltage and current waveforms at two different switching frequencies [3]

2.2 Resonant Power Converter

Resonant converter naturally contains *L-C* network whose voltage and current waveforms vary sinusoidal during one or more sub-intervals of each switching period. An *L-C* circuit can store electrical energy vibrating at its resonant frequency. A capacitor stores energy in the electric field between its plates, depending on the voltage across it, and an inductor stores energy in its magnetic field, depending on the current through it [2].

The resonant tank also serves as an energy buffer between input and the output, is normally synthesized by using lossless frequency-selective network. The purpose of that network is to regulate the energy flow from the source to the load [2]. Some types of resonant converters are:

1. DC-AC high frequency inverters
2. Resonant DC-DC converters
3. Resonant inverters or rectifiers producing line frequency AC

Resonant converter achieves very low switching loss thus enable resonant topologies to operate at switching frequency. There are 3 types of resonant topologies:

1. SRC (series resonant converter)
2. PRC (parallel resonant converter)
3. LLC/SPRC (series-parallel resonant converter)

These topologies differ in the arrangement of the resonant tank (consist of *L* and *C*). The DC characteristic of *LLC* converter is like a flip of DC characteristic of *LCC* resonant converter. For a resonant tank, working at its resonant frequency is the most efficient way. This rule applies to SRC and PRC very well. For *LCC*, it has two resonant frequencies. Normally, working at its highest resonant frequency will be more efficient [2].

2.2.1 Losses in Power Converter

There are three major losses in power converter such as:

1. Conduction and switching losses in power switches.
2. Losses due to charging and discharging stray component in a power converter.
3. Losses in a controller

a) Switching loss

In resonant switching circuits, switching takes place when voltage and/or current are zero. Thus simultaneous transitions of voltage and current are avoided. This type of switching is called “soft switching” .There two types of switching losses which at turn-on and turn-off of the inverter circuit. During turn-on, the switching loss is mainly caused by the dissipation of energy stored in the output parasitic capacitor of the power switch. During turn-off, the power transformer leakage inductance produces high *di/dt*, which results in a high voltage spike across it [8]. Zero-voltage switching also reduces converter-generated electromagnetic interferences (EMI). Zero-current switching can be used to commutate silicon control rectifier (SCR) [2].

By using high switching frequency in power electronic devices, it allows more space area on board due to the smaller physical size and value of the components, smaller output inductance value, and wider control bandwidth [5]. However, by increasing the operation frequency, this will also increase the switching loss and reduce the system efficiency [2]. Therefore, the rise and the fall time need to be determined properly according to the parameters in the datasheet. This can be proven by equation (1) below

$$P_{sw} = \frac{1}{2} t_{sw} P_{peak} f_{sw} \tag{1}$$

The switching loss can be reduced by two ways that are faster switching time and/or lower the *I-V* product during transition cycle [5]. The ideal switching loss illustration is as shown in figure 3 where the overlapping of the voltage and current waveform produces power loss as applied in equation above.

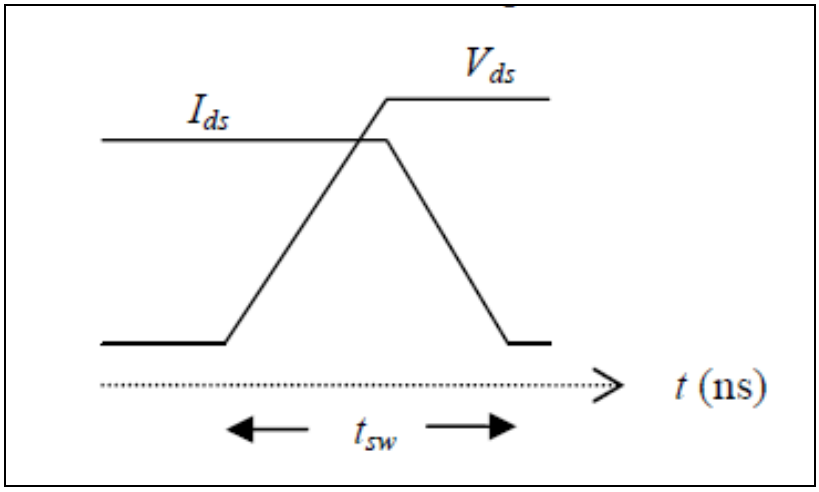


Figure 3: Ideal switching loss (*I-V*), [5]

Another solution of reducing the switching loss is by using the resonant network. Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions which will reduce the switching loss due to the current through or voltage across switching device at switching point near or equal zero[2]. The reduction in switching losses allows the designer to attain higher operating frequency without reducing converter efficiency, and using small-size and low-weight converters [5].

When varying the switching frequency with the resonant frequency, the switching current waveform and resonant inductor current change [2]. Besides that working in high switching frequency $(f_s > f_r)$ will contribute to high switching loss. Figure 4 below show the effect to the current waveforms when varying the switching frequency to be greater or equal with the resonant frequency.

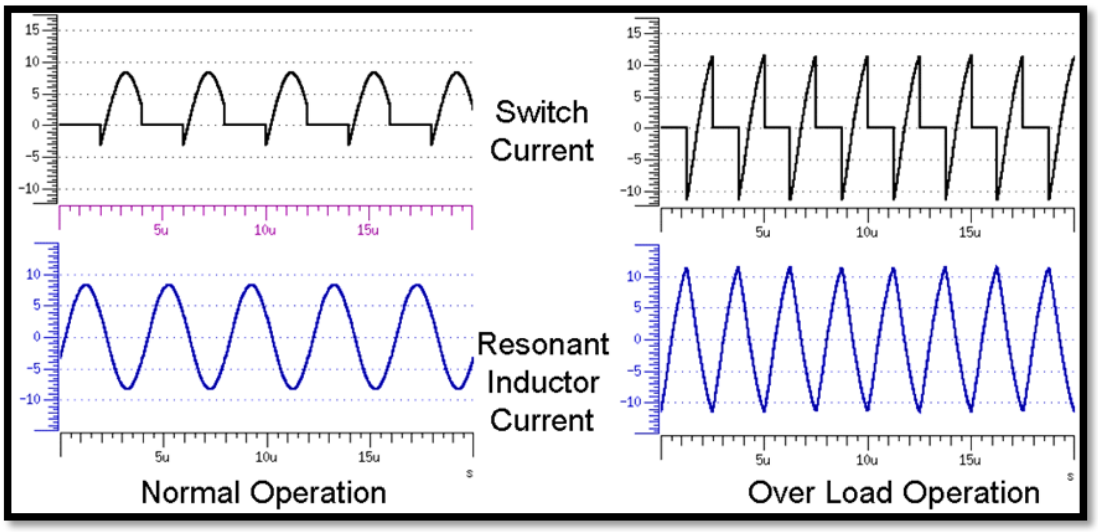


Figure 4: Effects to current and waveform when varying $f_s > f_r$ [2]

b) Conduction Loss

When a switch is off, normally a leakage current through the switch is very small and the energy loss being ignored along with the off-state. But when the switch is on, the energy loss depends on current through the switch and a forward voltage of the switch. This type of energy loss is called conduction loss of the switch [3].

Assuming that the on and off switching times are small compared to switching cycle, $T_{sw,}$ and the leakage current is negligible, I_{off} = 0. Thus the conduction loss is given by equation (2) below:

$$\bar{P}_{cond} = V_{on} \times I_{on} \times D \tag{2}$$

$$D = \frac{T_{on}}{T_{SW}} \tag{3}$$

Where T_{on} is the time when the switch is in on-state, V_{on} is a voltage drop across the switch, I_{on} is a current through the switch assuming it is constant in magnitude and D is a duty cycle. The duty cycle is based on equation (3) above. The switching loss should be calculated based on instantaneous current and voltage waveforms [3].

c) Dead Time Delay and Cross Conduction

The t_d is one of the limiting factors in high switching frequency applications. Referring to figure 5 below, dead time delay (t_d) is provided to prevent gate voltage of both MOSFETs from conducting. It is also used to avoid shoot through currents from supplied voltage to ground. If t_d is applied too long, this will introduce losses due to body diode conduction or else capacitive losses will be generated [5].

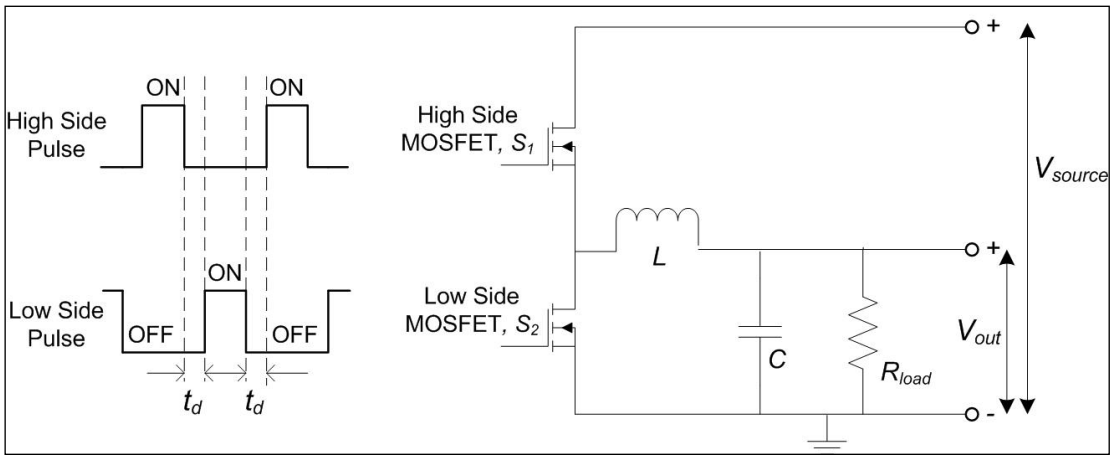


Figure 5: Dead Time Interval in PWM Switching [5]

When frequency increases, obviously the effects on the cross conduction is significant. The gate voltage of S_2 switch can easily be induced with higher value than its threshold. Therefore, in this case, S_2 could turn on accidentally and cross conduction eventually leads to excessive power dissipation in both MOSFETs [5].

2.3 Inverter Concept

Traditionally, DC to AC inverters are used to fix DC source in producing symmetrical AC output voltages. The output voltages are produced at fixed or variable frequency and magnitude. Inverter circuits are used to deliver power from a DC source to a passive or active AC load employing conventional SCRs or gate-driven semiconductor devices such as IGBTs, BJTs and MOSFETs. Apart from that, inverters are divided into voltage-source inverters and current- source inverters [4]

The inverters are used in applications where the only source available is a fixed DC source. The system requires an AC load such as uninterruptible power supply (UPS) application where DC to AC inverters are used for aircraft power supplies and variable speed AC motor drives. Apart from that, an inverter is used to regulate the speed of an induction motor and in a UPS system to produce a fixed AC frequency output the main power grid system is out [4].

2.3.1 Basic Inverter Circuit

To illustrate a basic concept of inverter circuit, we consider a half-bridge voltage-source inverter circuit. The circuit operation is very simple. The S_1 and S_2 on-off alternately as shown in figure 6 below. The circuit generates a square AC voltage across the load from constant DC source. The splitting capacitors are used to produce two equal voltages for turn-on and turn-off purpose. One observation to be made here is that the frequency of the output voltage is determined by the switching frequency. Apart from that, as mentioned earlier the switch can be replaced by MOSFETs, IGBTs and BJTs [4].

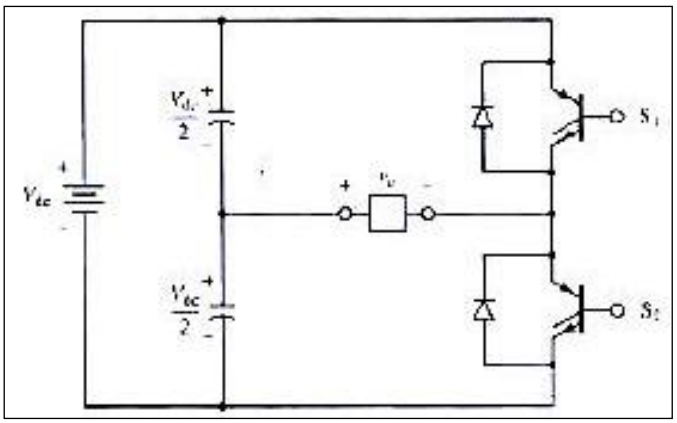


Figure 6: Half- bridge inverter circuit with large splitting capacitors [8]

2.3.2 Phase shift-PWM full bridge inverter

Full bridge inverter with series load as shown in figure 6 below achieves a soft switching state by tuning the operation frequency at the resonant frequency. The operating frequency refers to the switching frequency. Operating the inverter at the resonant frequency leads that the output total power factor of the inverter is close to 1, which reduces the conduction loss in the switching devices and the passive components that is occurred by the reactive current [6].

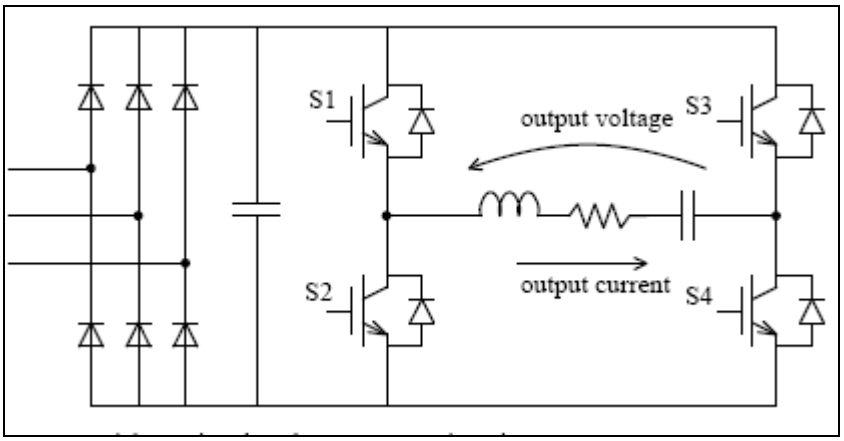


Figure 7: Full bridge inverter with series load resonant [6]

Apart from that, figure 8(a) and 8(b) below shows output waveforms of the resonant circuit. The output current waveform is assumed sinusoidal because it flows through the resonant circuit. Gate pulses that can determine the operating frequency through period time of the pulses as well as the duty cycle generate the input signals from the switches. As you can see, the output current leads when the operating frequency is lower than the resonant frequency. In this condition, the integration value of the output current becomes negative. Conversely, the integration value of the output current will become positive when the operating frequency is higher than the resonant frequency. The current phase becomes delay [6].

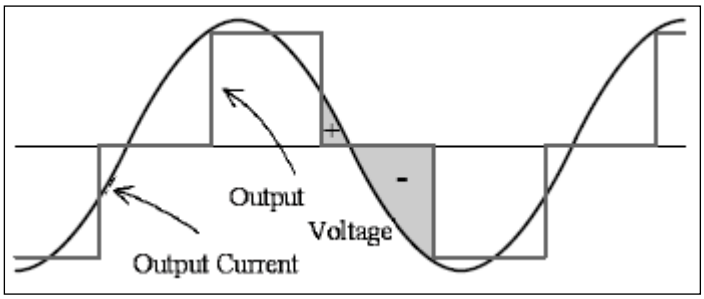


Figure 8 (a): Operating frequency lower than resonant frequency [6]

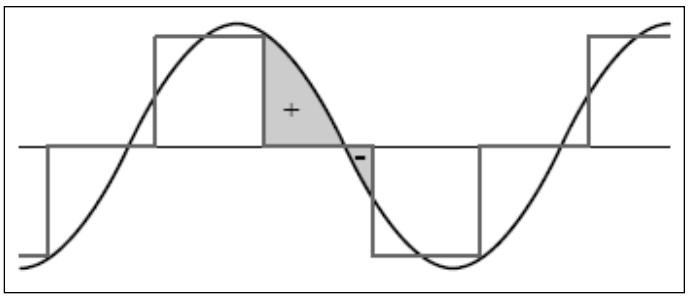


Figure 8 (b): Operating frequency higher than resonant frequency [6]

2.3.3 Full Bridge Series-Parallel Resonant Inverter

Figure 9(a) below shows the full-bridge series–parallel resonant inverter, which consists of four MOSFETs and the resonant network $LC_sC_pR_i$, where R_i is the equivalent resistance. The transistors are driven by gate source voltages V_{gs1}, V_{gs2}, V_{gs3} and V_{gs4}, which generate the conduction of M1 and M4 alternately to the conduction of M2 and M3, so that the full-bridge topology applies a square-wave voltage, V_{AB1}, to the resonant network. The waveforms in the resonant circuit are nearly sine waves, so essentially a sine wave appears at V_{AB1}. This analysis method is called the fundamental approximation [7].

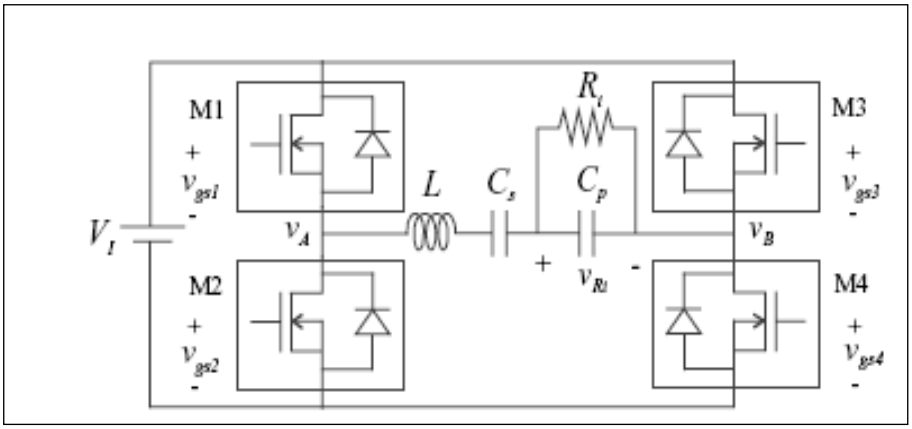


Figure 9(a): Resonant inverter circuit [7]

In figure 9(b), the equivalent impedance, Z_i, determines the operation mode. At the resonant frequency of the resonant tank, f_r, this impedance is purely resistive and the resonant current, I_L, is in phase with V_{ab1}. For ($f_r > f_s$), the series–parallel circuit represents a capacitive load, hence the current I_L leads V_{AB1}, and for ($f_r < f_s$), the resonant circuit represents an inductive impedance and the current I_L lags the voltage V_{AB1}, so transistors turn on at zero voltage and switching losses are null. This operation mode is known as zero voltage switching, (ZVS) [7].

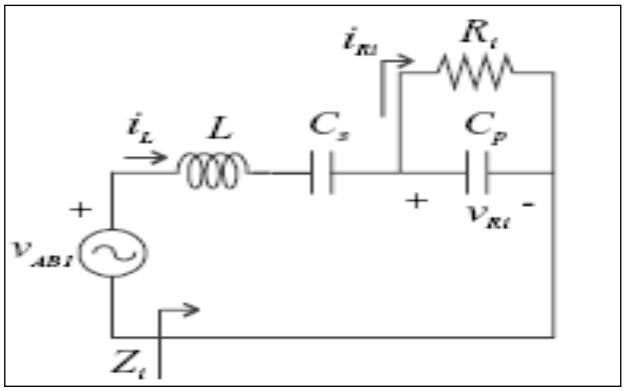


Figure 9(b): Simplified resonant tank [7].

2.3.4 Full bridge Inverter with Resistive and Inductive load

The full-bridge converter in figure 10 below is the circuit used to convert DC to AC. The ac output is developed from a DC input by closing and opening switches in an appropriate sequence. The output voltage V_o can be $+V_{DC}$, $-V_{DC}$, or zero, depending on which switches are closed. The full-bridge inverter produces a square-wave output voltage with a simple switching scheme. When M1 and M3 conduct, the switches connect the load to $+V_{DC}$. When M2 and M4 are closed, the switches connect the load to $-V_{DC}$. The periodic switching of the load voltage between $+V_{DC}$ and $-V_{DC}$ produces a square-wave voltage across the load. The output is alternating but non-sinusoidal. The current waveform is sinusoidal accordance to the voltage waveform. Figure 11 below shows the output waveforms of the inverter circuit. [8]

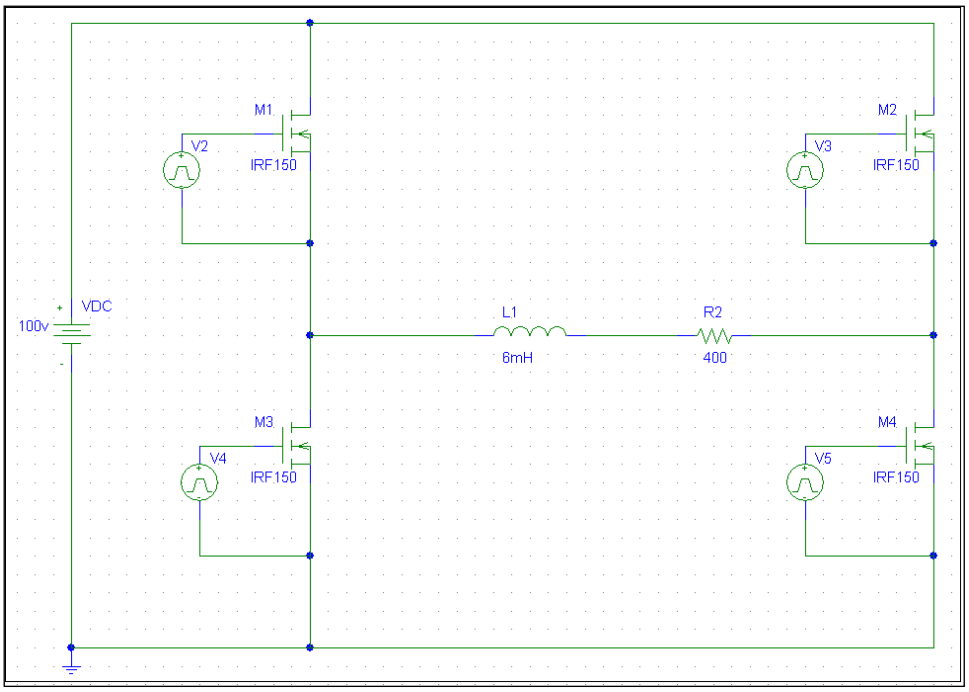


Figure 10: Full Bridge Inverter with Resistive and Inductive load

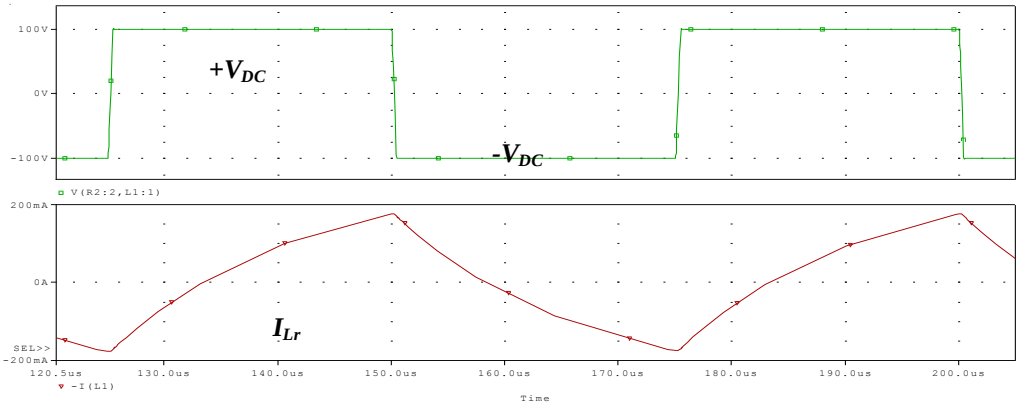


Figure 11: Voltage and Current Output Waveform [8].

2.4 Gate Pulse Implementation

Figure 12 below shows the timing PWM pulse sequence for a high frequency inverter. These voltages are supplied to the power semiconductor-switching block such as diode. Duty ratio defined as D=ton/T serves as a control variable for continuous power regulation for the inverter. Duty factor is designed as a ratio of the conduction time including a dead time of the main active power switches during a period. When the full power is delivered to the load, the conduction time of the main active power switch during one cycle is lengthened as indicated in figure 12 (a). On the other hand, when the full power is not required for load, the conduction interval is shortened as indicated in Figure 12 (b) [9].

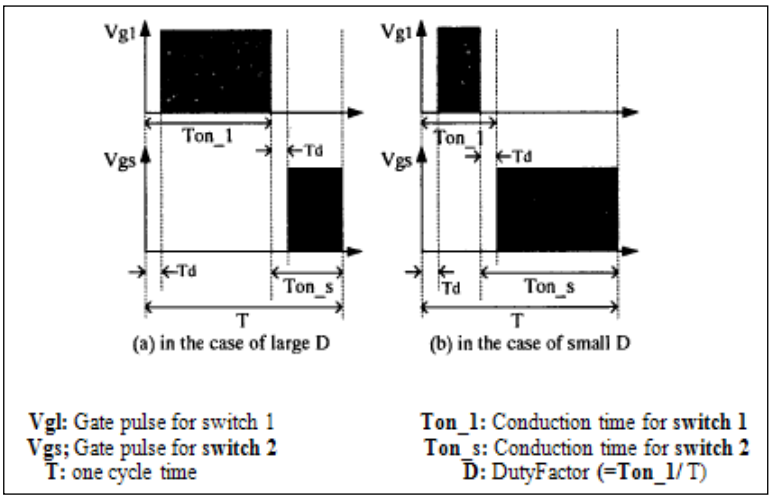


Figure 12: PWM gate pulse sequences [9]

2.5 Step Response of Series RCL Circuit

The series RCL circuit is known as second order circuit because their responses are described by differential equations that contain second derivatives. These step responses help student to find the initial and final conditions on circuit variables. Consider equation (4) below, applying KVL around the loop for t>0, [10]

$$L\frac{di}{dt} + Ri + v = V_s \tag{4}$$

But

$$i = c\frac{dv}{dt} \tag{5}$$

Substituting for i in equation (4) and rearranging terms,

$$\frac{d^2v}{dt^2} + \frac{R}{L}\frac{dv}{dt} + \frac{v}{LC} = \frac{V_s}{LC} \tag{6}$$

which has the same form as equation (6). More specifically, the coefficients are the same (and that is important in determining the frequency parameters) but the variable is different. Hence, the characteristic equation of the series RCL circuit is not affected by the presence of DC source. The solution to equation (6) has two components which are the transient response v_t (t) and the steady-state response v_{ss} (t) that is,

$$V(t) = V_s(t) + V_{ss}(t) \tag{7}$$

The transient response $v_t(t)$ is the component of the total response that die out with time[10]. Therefore, the transient response $v_t(t)$ for overdamped, underdamped and critically damped cases are:

$$v_t(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \quad \text{(overdamped)} \quad (8)$$

$$v_t(t) = (A_1 + A_2 t) e^{-\alpha t} \quad \text{(critically damped)} \quad (9)$$

$$v_t(t) = (A_1 \cos w_d t + A_2 \sin w_d t) e^{-\alpha t} \quad \text{(underdamped)} \quad (10)$$

The steady-state response is the final value of v(t).for inverter the steady-state response is the same as the source voltage v_s. Hence,

$$v_{ss} = v_s \quad (11)$$

Thus, the complete solutions for overdamped, underdam[ed, and critically damped cases are:

$$v_t(t) = V_s + A_1 e^{s_1 t} + A_2 e^{s_2 t} \quad \text{(Overdamped)}$$

$$v_t(t) = V_s + (A_1 + A_2 t) e^{-\alpha t} \quad \text{(Critically damped)}$$

$$v_t(t) = V_s + (A_1 \cos w_d t + A_2 \sin w_d t) e^{-\alpha t} \quad \text{(Underdamped)}$$

The values of constant A_1 and A_2 are obtained from initial condition: v(0) and dv(0)/dt. Keep that in mind that *v* and *i* are respectively the voltage across the capacitor and the current through the inductor. Therefore, equation above only applies for the finding of *v*. However, once the capacitor voltage is known we can determine the current that is the same for every load in series RCL circuit [10].

CHAPTER 3
METHODOLOGY

3.1 Procedure Identification

This project begins with some research work about converter and its component in the 'Fundamentals of Power Electronics' book. The project flow as below:

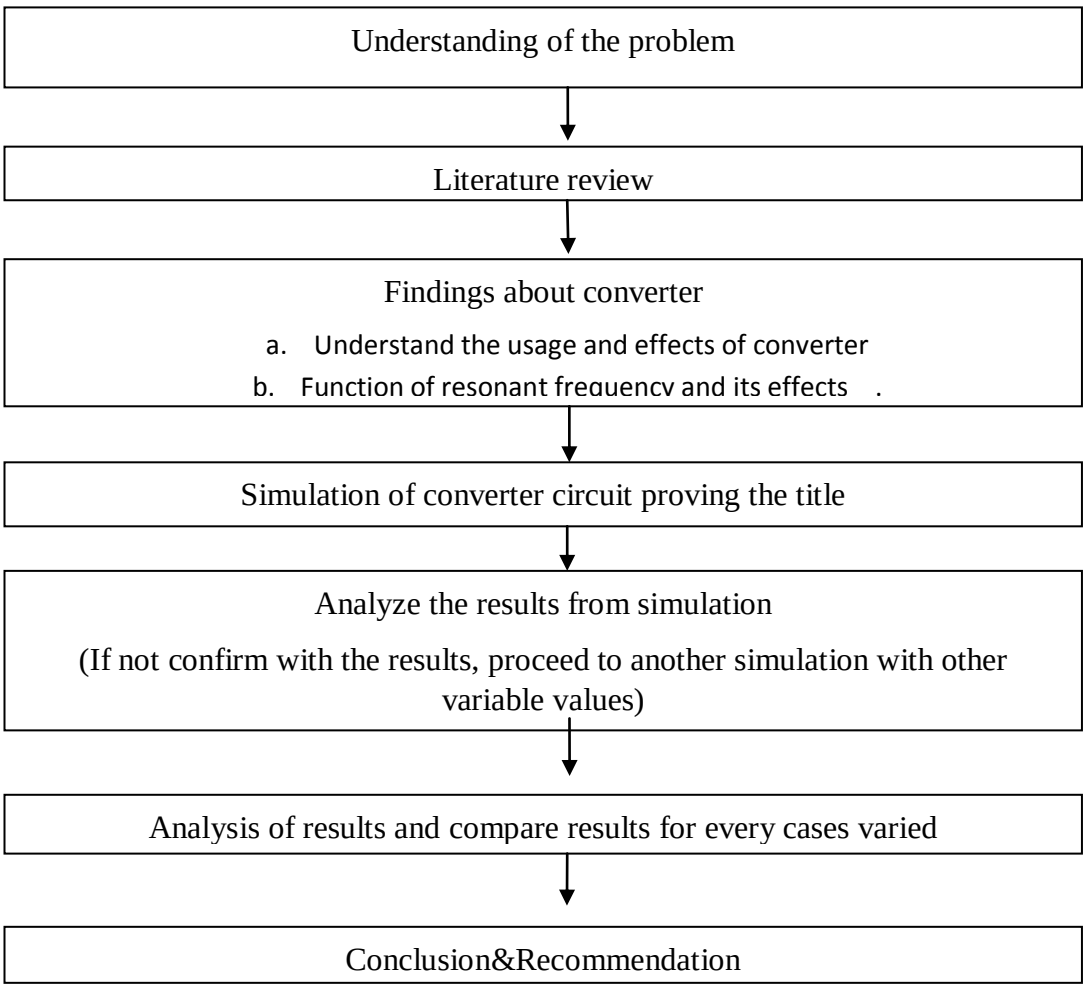


Figure 13: Project work flow diagram

3.2 Analysis Techniques

After getting familiar with the resonant inverter, the proposed circuit can be analyzed. The analysis technique can be done using:

1. PSPICE simulation to ensure getting the accurate value for each finding.

3.2.1 *Circuit Description*

Figure 14 below shows a Full bridge Inverter with RCL load in series. This circuit produces a square alternating waveform for the voltage output that is similar to the theory. It also produces a sinusoidal current waveform as the output. The switching frequency of 20 kHz generated through the voltage pulses that are connected through MOSFETs (M1, M2, M3 and M4). The resonant frequency is varied from 4.78 kHz until 100 kHz, which is based on the amount of resonant load connected in series .The resonant frequency, is calculated through formula.

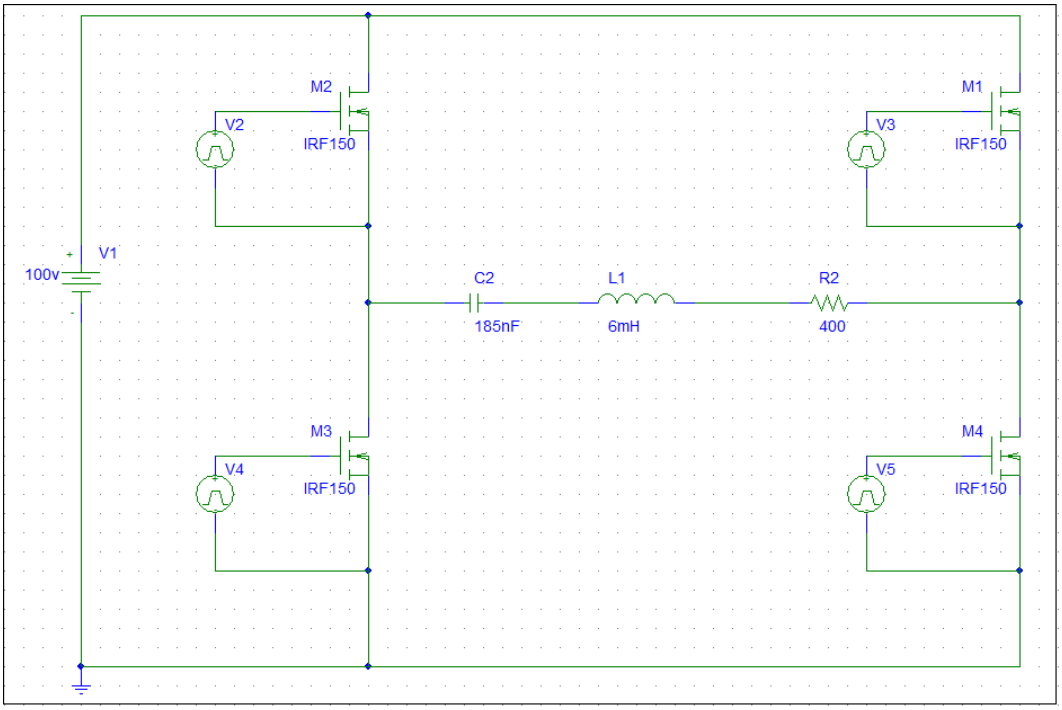


Figure 14: Full Bridge Inverter with RCL Load in Series

Basically the operations circuit begins when M1 and M3 are about to turn-on and *M2* and *M4* is turn-off. The following part in this chapter will prove that M1 and M3 conduct at the same time as well as M2 and M4.M1 will turn-on when the $V_{gs,\mathrm{M1}}$ reaches threshold voltage (V_{th}), at which point the drain current starts to flow and the gate voltage continues to conduct and drain current rises proportionally. This is based on transfer characteristic of MOSFET where V_{gs} increasing above V_{th}, I_{ds} start to conduct [8]. $V_{ds,\mathrm{M1}}$ then start to conduct in simultaneous manner when the $V_{gs,\mathrm{M1}}$ and $I_{ds,\mathrm{M1}}$ are turned-off. Same principle goes to turn-on the M2 of the MOSFET.

Circuit above consists of certain variables that are defined below:

a) Inductor (L1)

The inductor is a particularly troublesome component. Its high frequency equivalent circuit consists of several frequency dependent elements, including the inductance, inductor series AC resistance, as well as a parallel AC resistance. In parallel with the inductance is a small capacitor that represents the inter-winding capacitance. Below resonance, the inductor will behave as an inductor with increasing loss with increasing frequency. Above resonance, the inductor will behave as a capacitor, with decreasing loss at increasing frequency. Self-resonance can occur at a few hundred MHz for higher value inductors or can occur at a few GHz for smaller valued inductors. Below self-resonance, the inductor will behave as a low-pass filter, but above self-resonance, the inductor will behave as a high-pass filter [11].

b) Capacitor (C2)

The small signal equivalent of the capacitor consists of a series combination of the effective series inductance (ESL), the effective series resistance (ESR), and the bulk capacitance. Below resonance, it will behave as a capacitor, with a negative frequency dependent slope. Above resonance, it will have a positive impedance slope and will behave as an inductor [11].

c) MOSFETs

The MOSFET, either P-channel or N-channel will have an equivalent circuit that depends on whether the device is turned on or off. When the device is on, the equivalent circuit consists of a parallel combination of the drain to source resistance (R_{DS}), the equivalent output source to source capacitance, or C_{OSS} ($C_{OSS} = C_{gs} + C_{gd}$), and the body diode. When the switch is open R_{DS} becomes very large and so is not part of the equivalent circuit. Instead, the equivalent circuit consists of the C_{OSS} in series with its AC ESR. The body diode is modeled as an ideal diode, and becomes important if the DC bias of the junction turns the diode on and offers an alternative conduction path. In series with these will be the wire-bond inductance [11].

d) Pulse generator

The pulse is used to generate gate pulse signal to the respective MOSFETs. The gate pulse will determine the duty cycle of the circuit. Apart from that, the pulse generator is set as figure shown below. In this circuit, there are several factors affecting the performance and efficiency. Among them are the switching losses in between transition of M1 and M4, body diode conduction loss and the variation of dead time, t_d where the first two losses are directly related to the switching frequency. In this work, the fixed dead time scheme is used to avoid cross conduction and it was determined to be 15 ns. Figure 15 below shows the setting of the pulse generator in the PSPICE simulation.

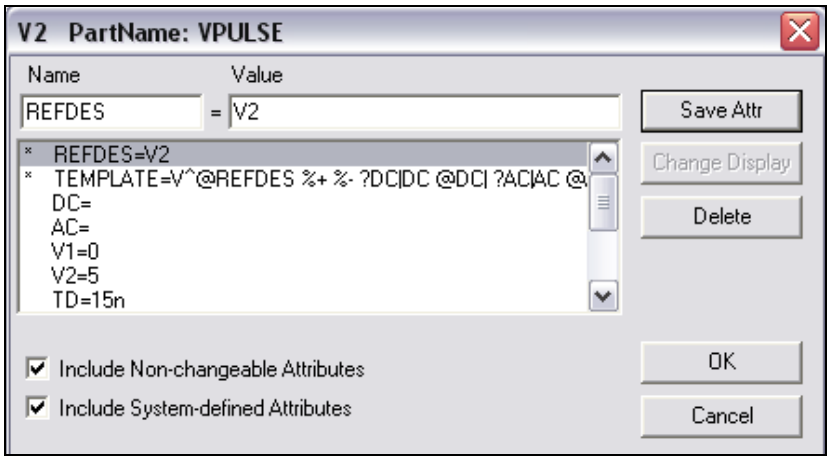


Figure 15: Setting for pulse generator

e) Voltage supply

Voltage supply is the power supply of circuit. It generates either DC or AC voltage to the circuit. The circuit above used DC voltage as a power supply.

f) Circuit parameters

Table 1, 2, 3 and 4 below shows the parameters of every component in the circuit for different value of resonant frequencies varied. Table 1 indicates that the resonant frequency is 4.78 kHz and table 2 shows resonant frequency of 30 kHz.

Table 1: Parameters for Full Bridge Inverter Circuit with RCL Load ($f_s > f_r$)

Voltage supply (V_{DC})	100 V
Resistor (R)	400 Ω
Inductor (L1)	6 mH
Capacitor (C2)	185 nF
MOSFETs (M1,M2,M3,M4)	IRF150 (rating 100 V,40 A,R_{DS}=0.055 Ω)
Switching frequency (f_s)	20 kHz
Resonant frequency (f_r)	4.78 kHz

Table 2: Parameters for Full bridge Inverter Circuit with RCL Load ($f_s<f_r$)

Voltage supply (V_{DC})	100 V
Resistor (R*)*	400 Ω
Inductor (L1)	6 mH
Capacitor (C2)	4.7 nF
MOSFETs (M1,M2,M3,M4)	IRF150 (rating 100 V,40 A,R_{DS}=0.055 Ω)
Switching frequency (f_s)	20 kHz
Resonant frequency (f_r)	30 kHz

Table 3 and 4 below is the parameter for the full bridge inverter circuit with RCL load where the value of the capacitor is varied to change the resonant frequency higher than 30 kHz for comparison purpose. The resonant frequency has to be varied to check out the impact of high resonant in the circuit itself.

Table 3: Parameters for Full Bridge Inverter circuit with RCL load ($f_s<f_r$)

Voltage supply (V_{DC})	100 V
Resistor (R)	400 Ω
Inductor (L1)	6 mH
Capacitor (*C2*)	1.7 nF
MOSFETs (M1,M2,M3,M4)	IRF150 (rating 100 V,40 A,R_{DS}=0.055 Ω)
Switching frequency (f_s)	20 kHz
Resonant frequency (f_r)	50 kHz

Table 4: Parameters for Full Bridge Inverter circuit with RCL load (f_s<f_r)

Voltage supply (V_{DC})	100 V
Resistor (R)	400 Ω
Inductor (L1)	6 mH
Capacitor (C2)	422 pF
MOSFETs (M1,M2,M3,M4)	IRF150 (rating 100 V,40 A,R_{DS}=0.055 Ω)
Switching frequency (f_s)	20 kHz
Resonant frequency (f_r)	100 kHz

g) Calculation

All the values obtained to complete the tables above are done through calculation. The inductor value has been assumed 6 mH in each frequency variation. The switching frequency for each circuit remains constant for this project except the resonant frequency. The resonant frequency is calculated using equation (12) below.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

When L=6 mH, we can change the value of the capacitor by varying the resonant frequency that being discussed in this project.

h) Gate pulse implementation

Figure 16 below shows the gate pulses generated to the inverter circuit. These voltage pulses are generated to the MOSFETs. We can set the duty cycle that associates with the switching frequency. Figure below shows the operating waveforms of Full Bridge Inverter with series RCL load circuit that clearly indicate that $V_{gs,M1}$ and $V_{gs,M3}$ conduct simultaneously with $V_{gs,M2}$ and $V_{gs,M4}$.

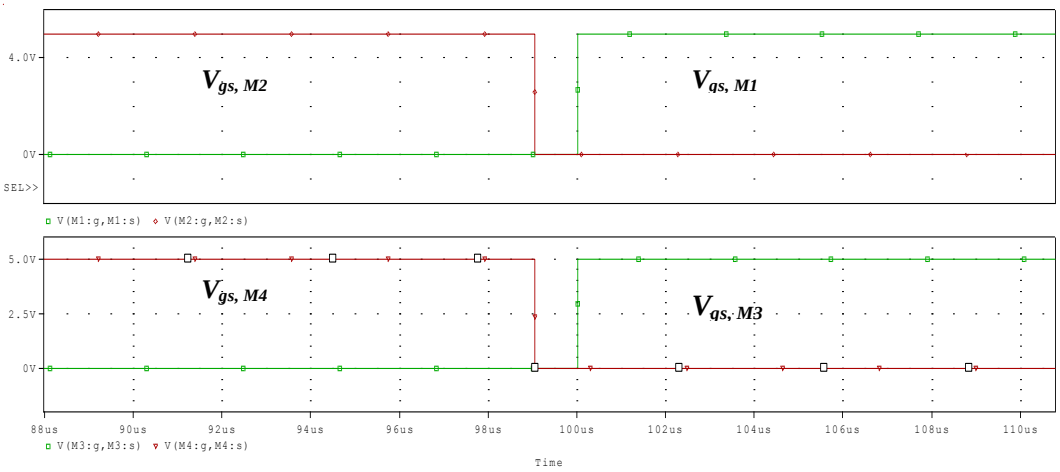


Figure 16: Operating Waveform of V_{gs} for M1, M2, M3 and M4 MOSFETs

Figure 17 below shows that there is no overlapping between V_{gs1} and V_{gs2} by providing suitable time delay to the gate voltages. If overlapping occurs, it will lead to cross conduction that enhances excessive power dissipation in both MOSFETs. The time delay for this circuit is 15 ns.

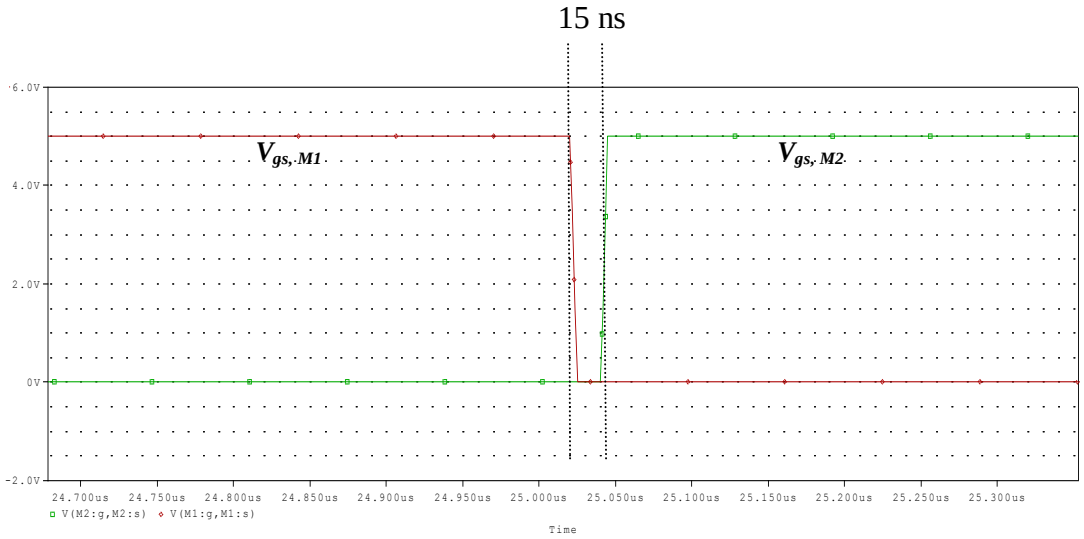


Figure 17: waveform of $V_{gs,M1}$ and $V_{gs,M2}$

3.3 Tools and Equipment Required

a) PSPICE student version 9.1

CHAPTER 4
RESULTS AND DISCUSSIONS

4.1 Simulation Results and Analyses

We have to get the fundamental results for the inverter before doing comparison. The simulation results should be the same as inverter application theory. The full bridge inverter is simulated to ensure all the settings are correct before we can proceed with comparing the resonance level in the circuit. These MOSFETs (M1, M3) and (M2, M4) are in turn conducting complementary to each other.

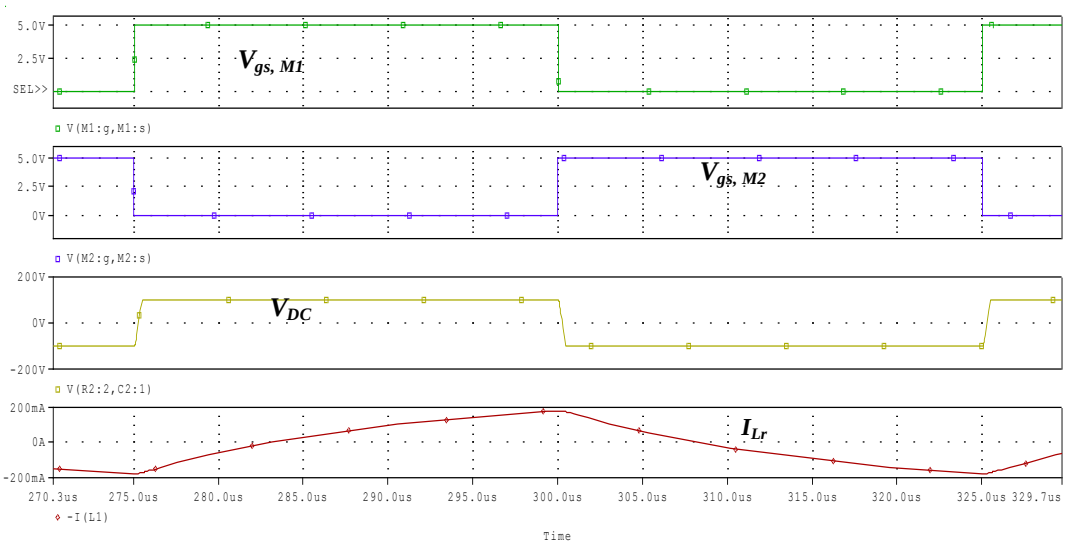


Figure 18: Output Voltage and Current for Full Bridge Inverter with RCL Load

The output voltage waveform is a square alternating waveform with $+V_{DC}$ and $-V_{DC}$. This shows that the output voltage is in AC, which complies with the theory of inverter application. The inductor current, I_L is also alternating which comply to inverter application.

Figure above indicates that when M1 and M3 conduct, the current and the voltage will oscillate positively. The above waveforms are varied under 50% of duty cycle. Duty cycle plays a big role in the conduction period of the voltage pulses. The duty cycle determines the value of Pulse Width Modulator (PWM) which effect the time of switching. The value of the inductor current is the same as calculation from formula in the literature review section.

The switching frequency for all the parameters compared is fixed to *20 kHz*. The resonant frequency chosen in this simulation are *4.7 kHz, 30 kHz, 50 kHz* and *100 kHz*. Each of this value represent for case $f_r < f_s$, $f_r > f_s$, $f_r >> f_s$ and $f_r >>> f_s$. The simulation results for each case are shown below.

a) Case 1: $f_r < f_s$

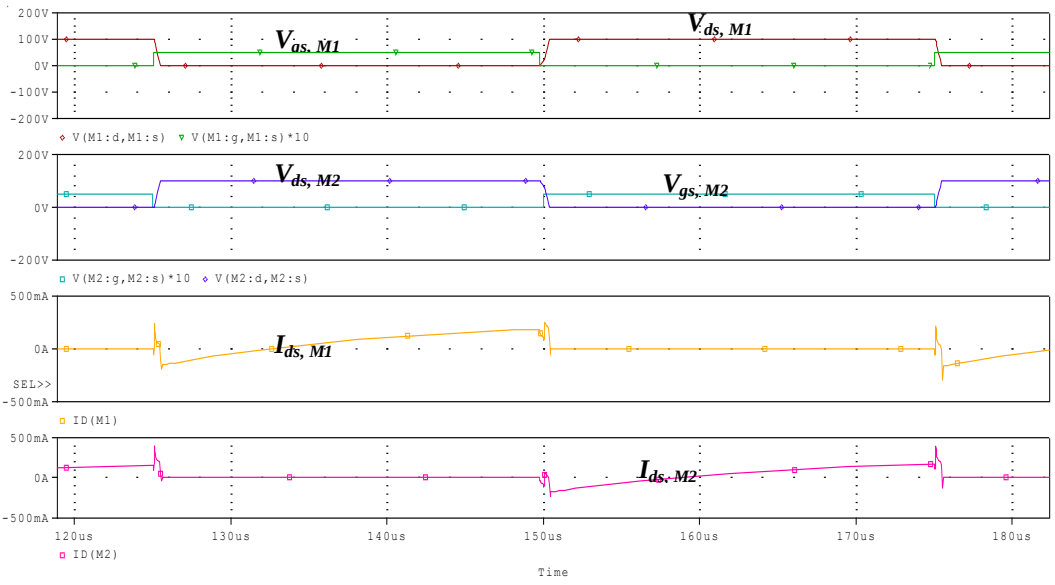


Figure 19: Operation Waveforms for f_r = *4.78 kHz*

For figure 19 above, it indicates that the gate voltages are working in non-ZVS mode. There are some differences according to the theory [5]. There is an overlapping at the starting of every conduction of $V_{gs,\ M1}$ and $V_{ds,\ M1}$ as well as $V_{gs,\ M2}$ and $V_{ds,\ M2}$ where cross-conduction occurs between those switches. However based on the theory

of MOSFET characteristics, supposedly V_{gs} and V_{ds} for both switches are not overlapping with each other due to ZVS mode [5]. Unfortunately, the gate voltages can be seen clearly, which comply with inverter application. Apart from that, there is no floating voltage during the conduction of V_{gs} and V_{ds} for both switches.

Non-ZVS mode occurs because of during turn-on for both switches as shown in figure 19, some stress already occurs at the switches causing the V_{gs} to switch-on before the V_{ds} can settle down properly. While during turn-off for both switches, the stress is absent, causing V_{gs} to switch-off properly before the V_{ds} start to rise. Since there are overlapping occur in the waveforms, therefore ZVS mode cannot be obtained [5].

Figure 20 below shows the current waveforms obtain are as desired after compare it theoretically [4]. Since *fr* < *fs*, the I_{ds} conduction meet the theoretical condition where I_{Lr} is in positive cycle when $I_{ds,M1}$ conduct and turn negative when $I_{ds,M2}$ conduct. During t_d, both switches are off ($V_{gs,S1}$ and $V_{gs,S2}$). At this point, the I_{ds} value or both switches reach its peaks value because of the V_{ds} reach its minimum value. There are at one point where both drain voltages of M1 and M2 conducting where $V_{ds,M1}$ increasing and $V_{ds,M2}$ decreasing [12]. This condition causing both drains current to decrease. The value of $I_{ds,M2}$ reaching the maximum negative value and the $I_{ds,M1}$ is completely turn-off. The next cycle of operation will repeat the same pattern of conduction mode.

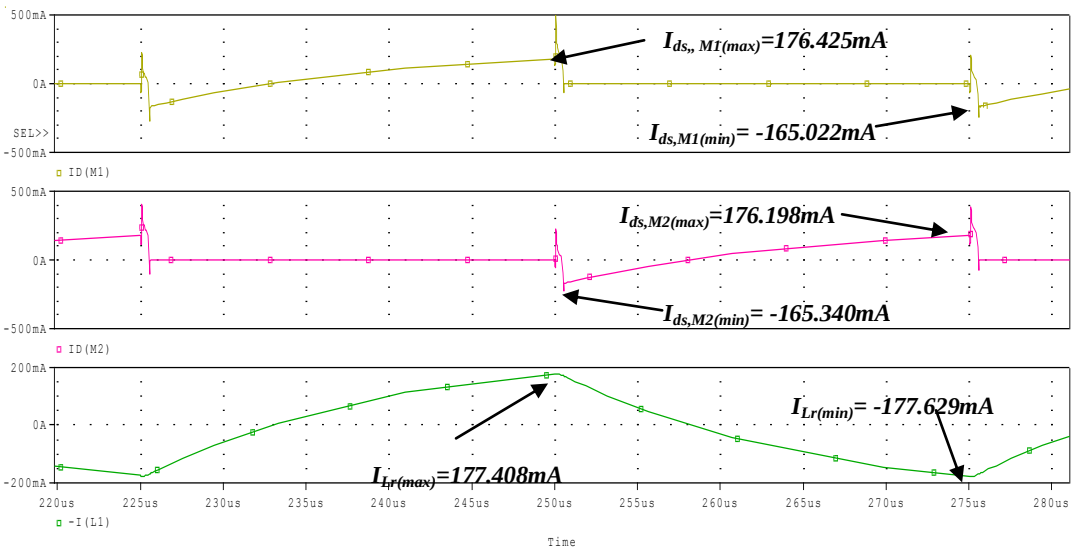


Figure 20 : Output Waveform for *fr=4.78 kHz*

b) Case 2: $f_r > f_s$

Figure 21 below shows the output voltage and current for inverter circuit itself when the resonant frequency is changed from *4.78 kHz* to *30 kHz*. The MOSFETs are driven by square-wave voltages V_{gs1}, V_{gs2}, V_{gs3} *and* V_{gs4}, which establish the conduction of M1 and M3 alternately to the conduction of M2 and M4, so that the full-bridge topology applies a square-wave voltage, V_{dc}, to the resonant network. As mentioned early, the figure below only shows the conduction of V_{gs1} and V_{gs2} because V_{gs3} and V_{gs4} have been proven to have the characteristics simultaneously. In this second case, the converter work in non-ZVS condition.

Figure 21 also shows that $V_{gs,\ M1}$ and $V_{ds,\ M1}$ are working in non-ZVS mode. The fixed dead time (t_d) of 15 ns can be seen between both waveforms before and after conduction. When V_{gs} for both switches is conducting, the I_{ds} will continuously charging and only start discharging when V_{gs} stop conducting and V_{ds} start conducting.

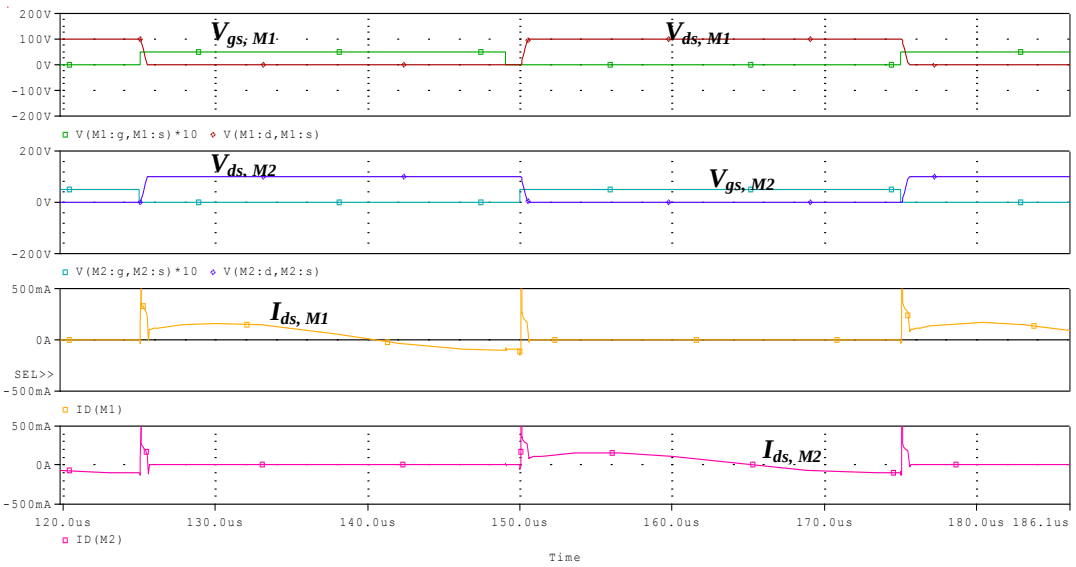


Figure 21: Operation Waveforms for *fr = 30 kHz*

The output result is the same compared to the theory that is an alternating wave of resonant current. The purpose of the resonant circuit is to filter the output voltage of the inverter, V_{DC}, to obtain sinusoidal voltage and current waveforms at the load. The resonant tank must provide the necessary steady-state load voltage and current with minimum resonant current to reduce switching losses. For $f_r > f_s$, the circuit represents a capacitive load, hence the inductor current leads the output voltage. According to the theory, the resonant load must provide with low resonant current in order to reduce switching losses. The figure 22 below shows that the resonant current is slightly lower compared to case $f_r < f_s$.

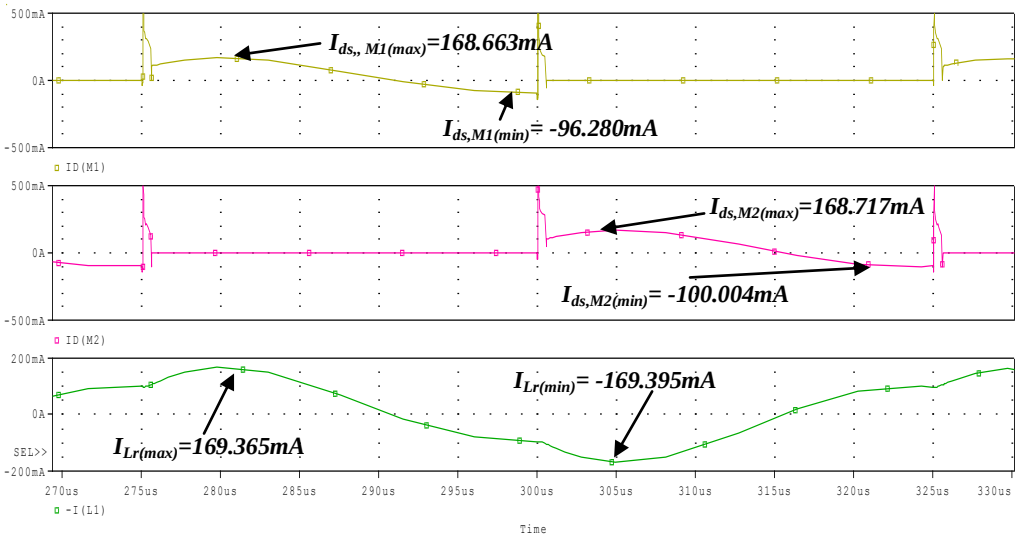


Figure 22 : Output Waveform for f_r=30 kHz

c) Case 3: $f_r >> f_s$

Figure 23 below shows the output voltage and current for inverter circuit itself when the resonant frequency is changed from *30 kHz* to *50 kHz*. For this case, the resonant current is working in ZCS mode. Figure below shows that $V_{gs,\,M1}$ and $V_{ds,\,M1}$ are working in non-ZVS mode. There is some difference according to theory. There is an overlapping at the starting of every conduction of $V_{gs,\,M1}$ and $V_{ds,\,M1}$. Unfortunately, the gate voltages can be seen clearly, which comply with inverter application. The reason for this problem to occur is due to low switching frequency and limitation of value assumed for the circuit.

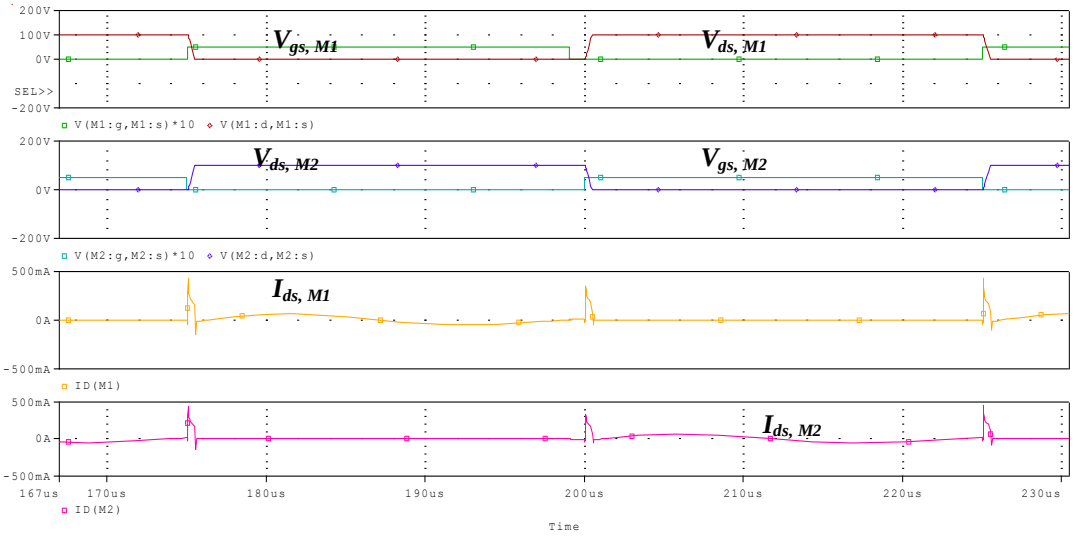


Figure 23: Operation Waveforms for f_r = *50 kHz*

Figure 24 below shows the inductor current is in ZCS mode. The inductor current is lower than the previous cases that have the chance to achieve low switching loss. The conduction of the diode follows the inverter concept. The resonant current is getting smaller.

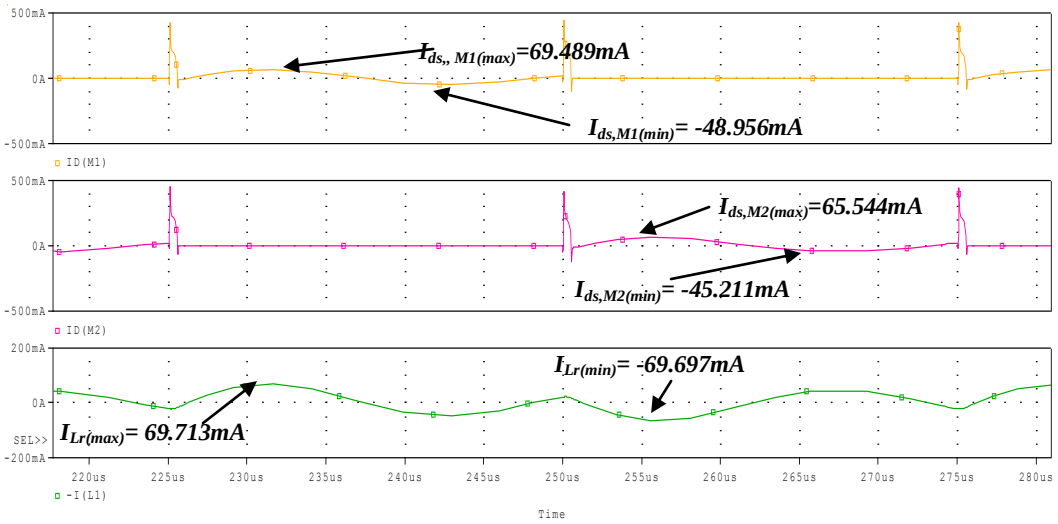


Figure 24 : Output Waveform for f_r=*50 kHz*

d) Case 4: $f_r >>> f_s$

Figure 25 below shows the output voltage and current for inverter circuit itself when the resonant frequency is changed from *50 kHz* to *100 kHz*. For this case, the inductor current is working in ZCS mode. Figure below shows that $V_{gs,\ M1}$ and $V_{ds,\ M1}$ are working in non-ZVS mode. There are double charging discharging when power switches conduct.

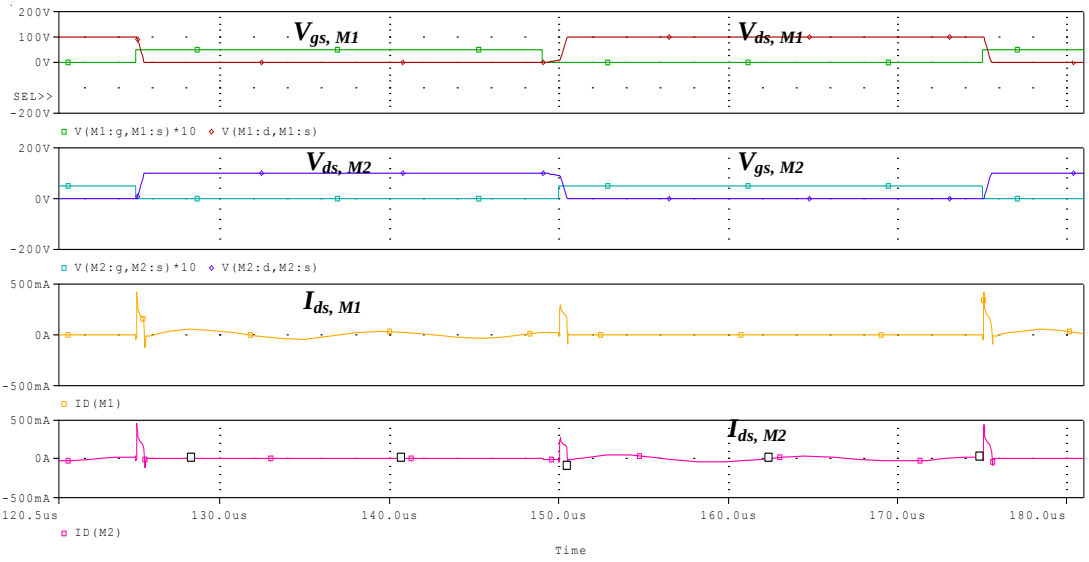


Figure 25: Operation Waveforms for f_r = *100 kHz*

The simulation results shown in figure 26 below do not comply with the fundamentals of inverter application. The resonant current is oscillating twice for one period of time that does not match with the theoretical result. The resonant current value is much even smaller than the previous case that can contribute to low switching loss but the oscillation of the current is doubtful and do not match the theoretical approach. Higher frequencies may damage the MOSFETs itself.

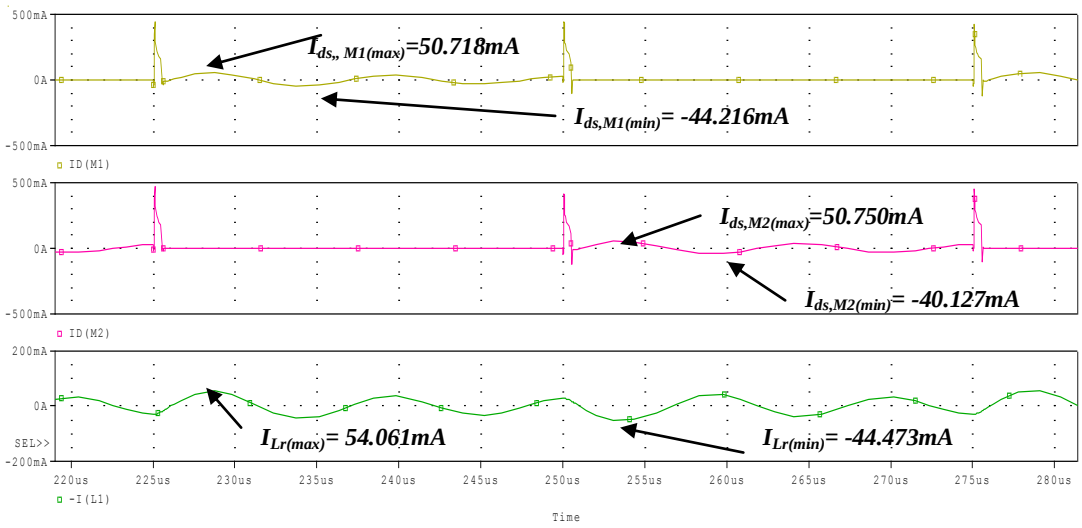


Figure 26 : Output Waveform for f_r=*100 kHz*

Table 5 below shows the conclusion in each result being discussed. From the table we can see that the inductor current matches the theoretical approach where maximum and minimum inductor current should be the same but differ in magnitude. The inductor maximum current, $I_{Lr(max)}$ and inductor minimum current, $I_{Lr(min)}$ for every frequency tabulated show slight error in the value finding. The inductor current value for *100 kHz* resonant frequency is unacceptable due to high percentage of error in the magnitude of maximum and minimum current. The circuit that varied with *50 kHz* of resonant frequency shows the best condition in this evaluation project. There is only a slight error compared to others.

Table 5: Inductor Current Comparison

Resonant frequency,f_r	Switching frequency,f_s	Inductor current,$I_{Lr(max)}$	Inductor current, $I_{Lr(min)}$	Error, (%)	Percentage of inductor current decrease (%)
4.78 kHz	*20 kHz*	177.408 mA	-177.629 mA	0.12	0
30 kHz	*20 kHz*	169.365 mA	-169.395 mA	0.02	4.53
50 kHz	*20 kHz*	69.713 mA	-69.697 mA	0.02	60.7
100 kHz	*20 kHz*	54.061 mA	-44.473 mA	17.7	69.5

From the table, we can conclude that decreasing of inductor current contributes to low switching loss. It also indicates that the inductor current is decreasing gradually with the resonant frequency. From the table, a graph that shows how the inductor current reacts with the resonant frequency is plotted.

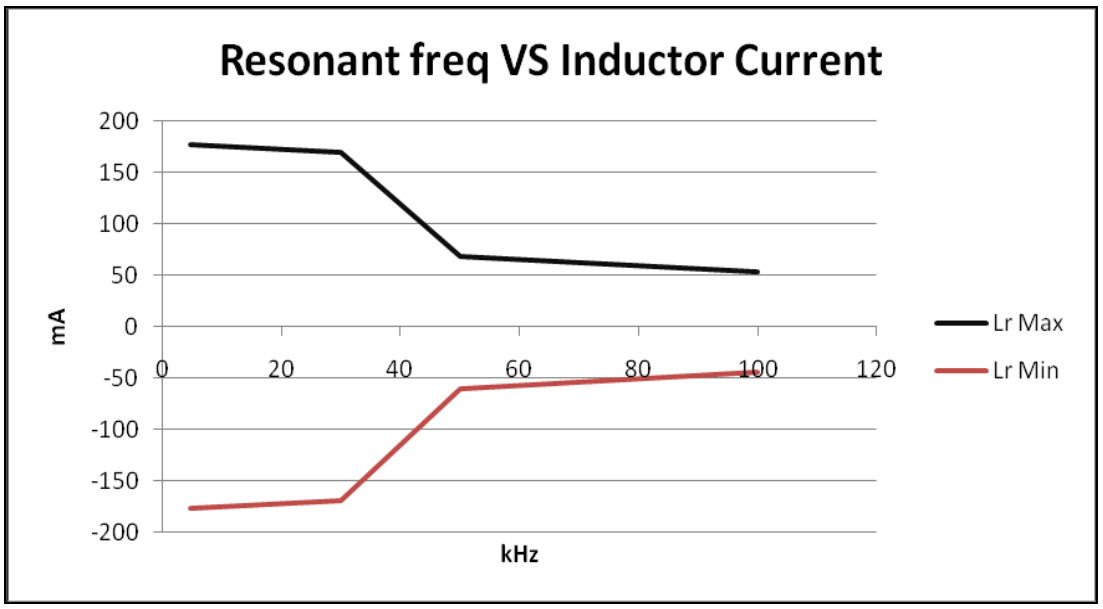


Figure 27: Graph of Resonant Frequency Vs Inductor Current

The figure 27 above shows the graph of inductor current when being varied with 4.78 kHz, 30 kHz, 50 kHz and 100 kHz. The minimum inductor current is exactly the as the maximum inductor current which shows that the circuit is correct. The above graph complies with the theoretical assumption. The above graph also shows that the inductor current is getting smaller with higher resonant frequency. This also shows that minimum resonant current can lead to reduction in switching loss where the V_{ds} value for M1, M2, M3 and M4 are constant to the $+V_{DC}$ value. According to theory of switching loss in [5], power peak switching value during turn-on and turn-off of switches is the multiple of V_{ds} and I_{ds}. When V_{ds} have a constant value, the smaller the I_{ds} value, the peak switching power will become smaller. However, the switching loss in this work cannot be obtained due to the waveforms that not satisfy the theory [5]. The area where I_{ds} and V_{ds} should intercept as shown in figure 28(a) and figure 28(b) below. Supposedly the I_{ds} and V_{ds} waveform should intercept with each other during turn-on and turn-off. Therefore, switching loss value cannot be drawn.

a) Case: $f_r < f_s$

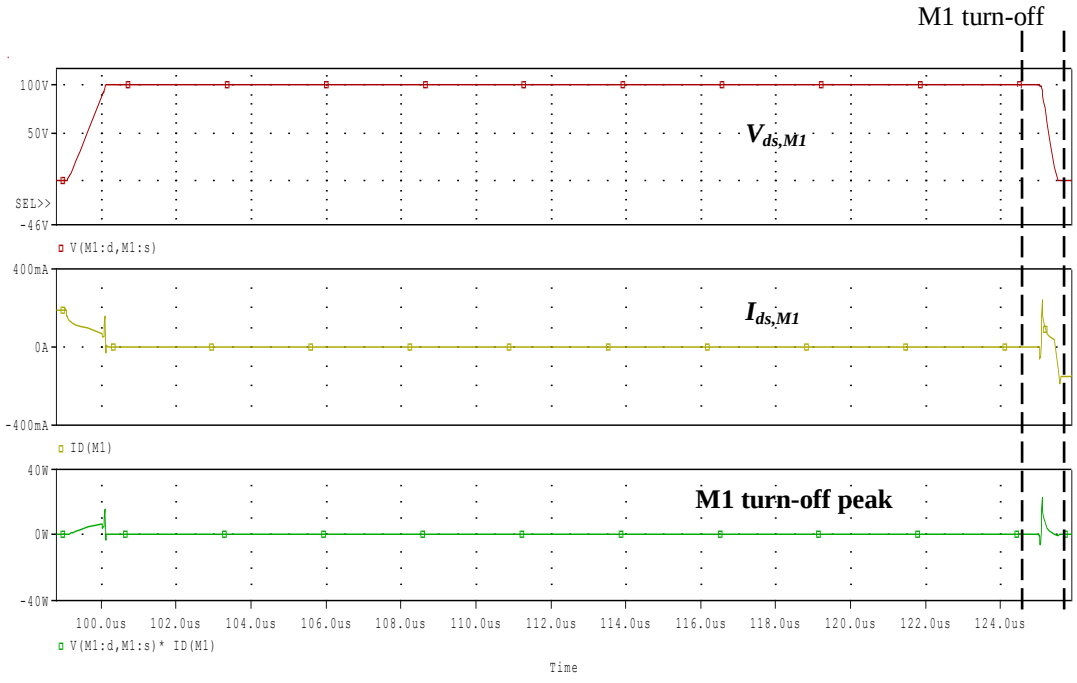


Figure 28(a) : Output Waveform during M1 turn-off

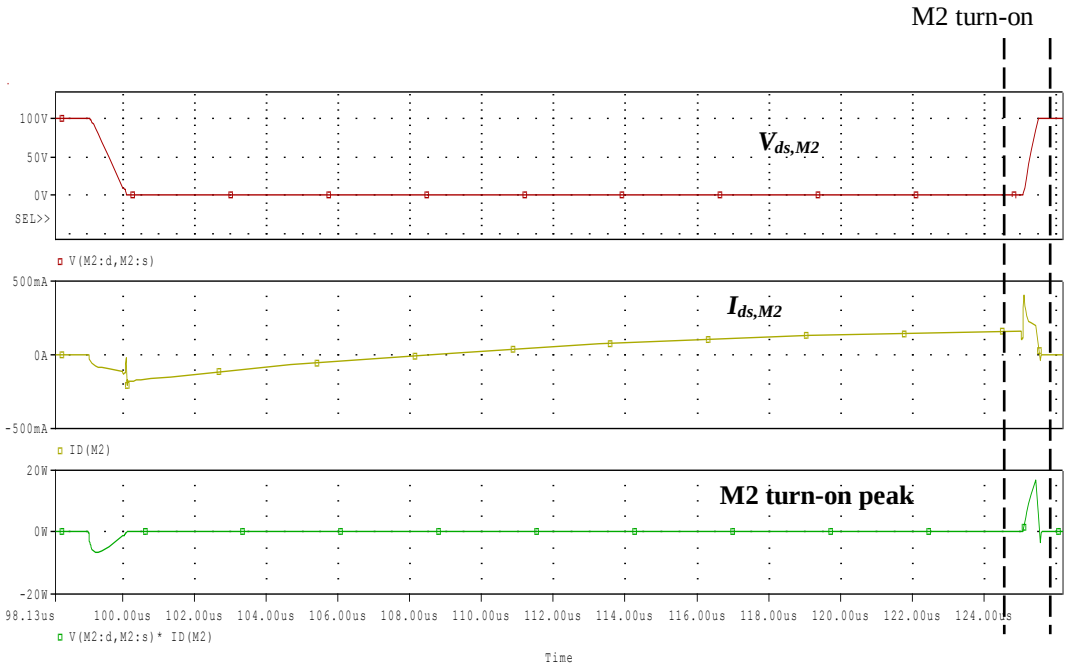


Figure 28(b) : Output Waveform during M2 turn-on

The switching for other cases also cannot be drawn due to the problem. The results for the remaining cases are attached in Appendix D.

As to conclude the results being discussed, the best circuit drawn from the analysis is RCL circuit with 50 kHz of resonant frequency. The circuit complies with all the inverter application and the resonant current is smaller compared to others. Although circuit with 100 kHz of resonant frequency has the least inductor current but the conduction of both I_{ds} and I_{Lr} of the circuit does not comply with the conduction theory in inverter application.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.1 Conclusion

Traditionally, DC to AC inverters used to fix DC source in producing symmetrical AC output voltages. The output voltages are produced at fixed or variable frequency and magnitude. The output voltage waveform is a square alternating waveform with $+V_{DC}$ and $-V_{DC}$. This shows that the output voltage is in AC and the inductor current, I_L also oscillates according to the conduction of diode. The above section also indicates that the resonant current is decreasing gradually with high resonant frequency. As a conclusion, the inverter circuit with *50 kHz* of resonant frequency serves the best condition when compared with other resonant frequencies discussed. Minimum resonant current contributes to reducing switching loss. The objective and scope of study of this project is achieved.

5.2 Recommendation

There are some recommendations for future work of this project:

- Try to use other MOSFETs as switching component that will not affect the switching performance. The switching loss of the circuit can be drawn if better switching component has been used.
- Try to analyse other type of resonant inverter such as series-parallel resonant inverter for comparison purpose. The comparison is done to see which circuit served the best in the same resonant frequency.
- Use experimental approach to prove the simulation being discussed.

REFERENCES

[1] R.W Erikson.(2004). *Fundamentals of Power Electronic* [Online].available: http://www.ieee.li/pdf/introduction_to_power_electronics/chapter_19.pdf

[2] Bo Yang.(2004). *LLC Resonant Converter*[online].available:http://scholar.lib.vt. Edu/theses/available/etd-09152003180228/ch4.pdf

[3] Firuz Zare, "EMI Issues in Power Electronic System," *IEEE Transaction on Power Electronics*, pp.66-70, 2009

[4] Issa Batarseh, "DC-AC Inverter*,"* in *Power Electronic Circuits,* Central Florida: John Wiley & Sons,2004, pp.400-437.

[5] N. Z. Yahaya, K. M. Begam and M. Awan, "Investigation Of High Frequency Effects On Soft-Switched Synchronous Rectifier Buck Converter " in IEEE Symposium on Industrial Electronics and Applications, October 4-6,2009,pp.524-528.

[6] Hiroyasu Kifune and Yoshihiro Hatanaka, "Resonant Frequency Tracking Control by Using One CT for High Frequency Inverter", *IEEE Transaction on Power Electronics* ,pp.1-7,2009.

[7] Rosario Casanueva, Francisco J.Azcondo,Salvador Bracho," Series–Parallel Resonant Converter for an EDM Power Supply," *Journal of material processing technology*, pp.172-175,23 October 2003.

[8] K.S Rama Rao, "Introduction to Resonant Conversion," unpublished

[9] Hideki Sadakata , Mutsuo Nakaoka , Hidekazu Yamashita , Hideki Omori and Haruo Terai, "Development of Induction Heated Hot Water Producer using Soft Switching PWM High Frequency Inverter", *IEEE Transaction on Power Electronics,* Vol 2 ,pp. 452-455,2002

[10] Alexander Sadiku," Step Responce," in *Fundamentals of Electric Circuit,* New York: Mcgraw Hill International Edition, pp.331-332,2007.

[11] Micheal Laflin(2006).HighFrequency Implications for Switch-mode DC - DC Converter Design[online].available: http://www.enpiron.com/Collateral/Documents/ English-US/High-frequency- implications-for-switch-mode-DC-R_0.pdf

[12] Eric Persson(2008).Optimizing Synchronous Buck Converter Efficiency InternationalRectifierCorp[online].available:http://www.powerdesignindia.co.in/STATIC/PDF/200810/PDIOL_2008OCT22_SUPPLY_TA_02.pdf

APPENDICES

APPENDIX A

GANTT CHART FYP 1

	PROJECT ACTIVITIES	WEEK													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	• Project/Topic Selection														
2	• Data Gathering • Research and discussion on topic • Preparation for preliminary report														
3	• Research on Resonant Converter. • Define objective and scope of study. • research on Inverter concept														
4	• Get to know about PSPICE simulation. • Research on high frequency inverter														
5	• Update on literature review														
6	• Submission of preliminary report.														
7	• Seminar 1.														
8	• Simulation of circuit and graph identification														
9	• Read books regarding project. • Update literature review. • Preparation and data gathering for final report and interim report.														
10	• Submission of Final Draft Report	21st October 2009													
11	• Submission of Interim Report	30th October 2009													
12	• Oral Presentation	30th November - 4th December 2009													

APPENDIX B

GANTT CHART FYP 2

	PROJECT ACTIVITIES	WEEK													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	• verify the suitable circuit to be used for simulation • Preparing report for Progress Report 1														
2	• simulation in progress														
3	• Preparing report for Progrest Report 2														
4	• simulation in progress														
5	• result obtained from simulation and being discussed														
6	• study on the results obtained														
7	• Preparing report for Draft and Final Report (Soft Cover)														
8	• Submission of Technical Report	5th May 2010													
9	• Submission of Final Report (Soft Cover)	5th May 2010													
10	• Submission of Final Report (Hard Cover)	25th June 2010													
11	• Oral Presentation	7th June - 11th June 2010													

APPENDIX C

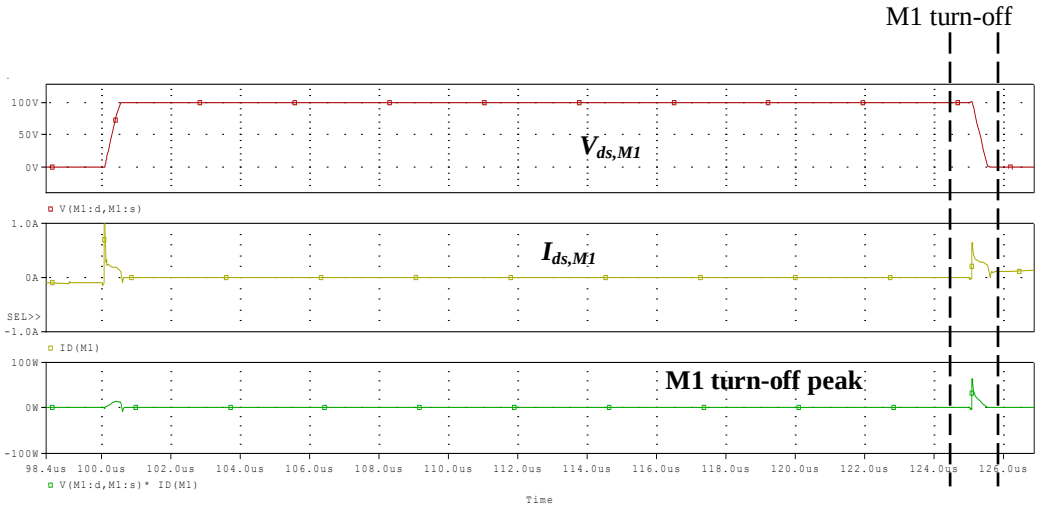
DATASHEET-IRF 150 DATASHEET

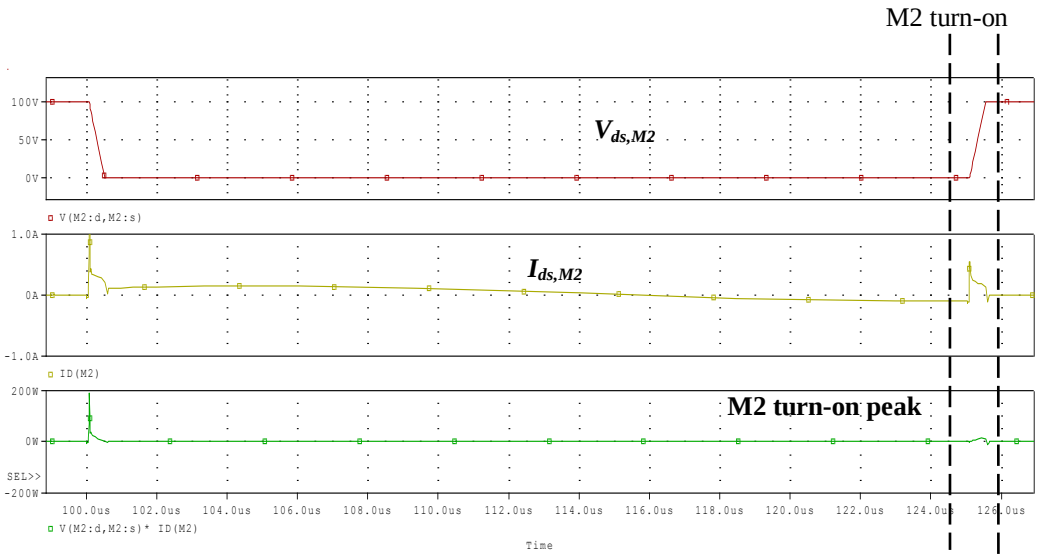
APPENDIX D

RESULTS FOR SWITCHING LOSS (*I-V* INTERCEPTION)

Case: $f_r > f_s$

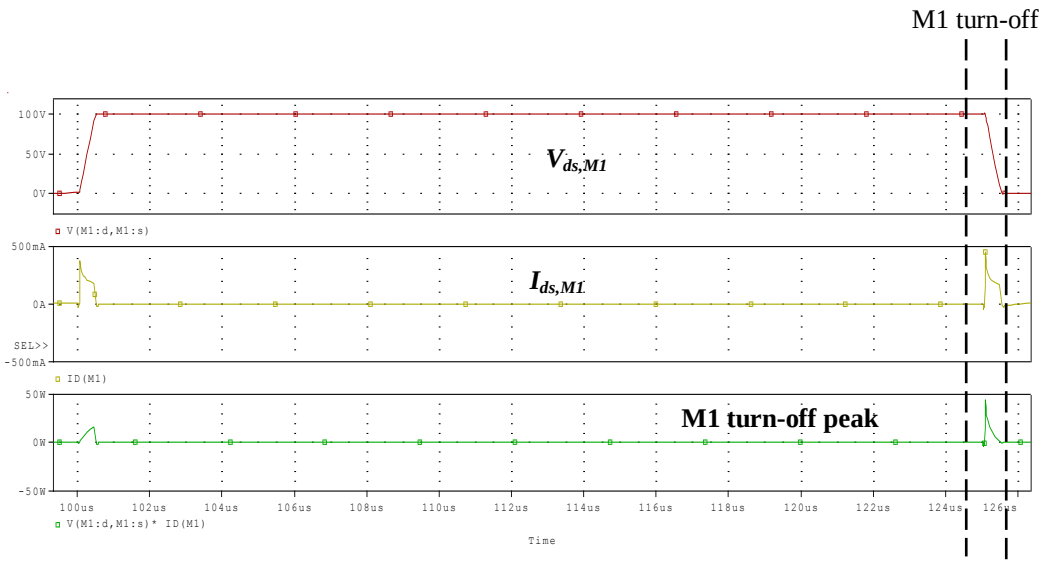
f_r = 30 kHz and f_s = 20 kHz

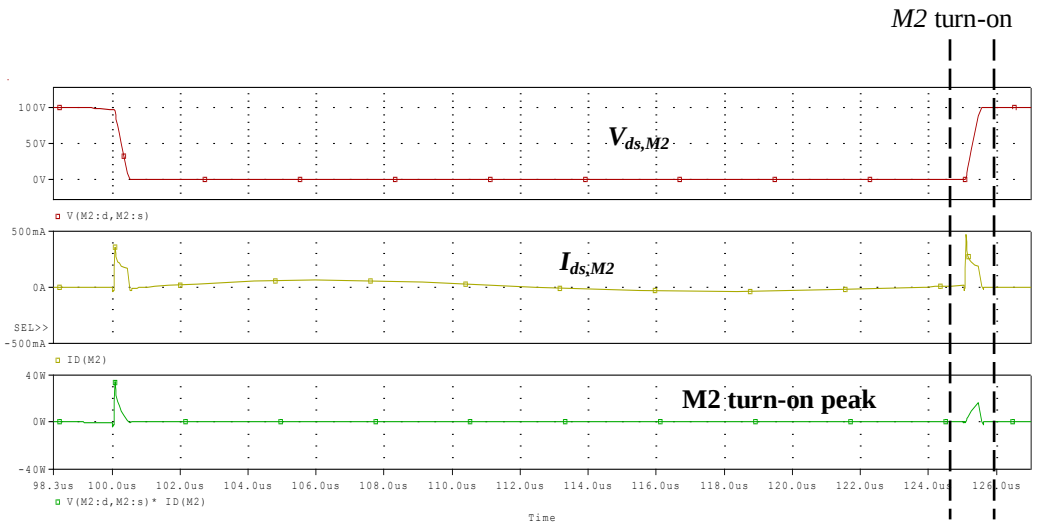




Case: $f_r >> f_s$

f_r = 50 kHz and f_s = 20 kHz





Case: $f_r >>> f_s$

f_r = 100 kHz and f_s = 20 kHz